

Self-Protected Low Side Driver with In-Rush Current Management

NCV8412, NCV8412D

The NCV8412 is a three terminal protected Low-Side Smart Discrete FET. The protection features include Delta Thermal Shutdown, overcurrent, overtemperature, ESD and integrated Drain-to-Gate clamping for overvoltage protection. The device also offers fault indication via the gate pin. This device is suitable for harsh automotive environments.

Features

- Short-Circuit Protection with In-Rush Current Management
- Delta Thermal Shutdown
- Thermal Shutdown with Automatic Restart
- Overvoltage Protection
- Integrated Clamp for Overvoltage Protection and Inductive Switching
- ESD Protection
- dV/dt Robustness
- Analog Drive Capability (Logic Level Input)
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Grade 1 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

Typical Applications

- Switch a Variety of Resistive, Inductive and Capacitive Loads
- Can Replace Electromechanical Relays and Discrete Circuits
- Automotive/Industrial

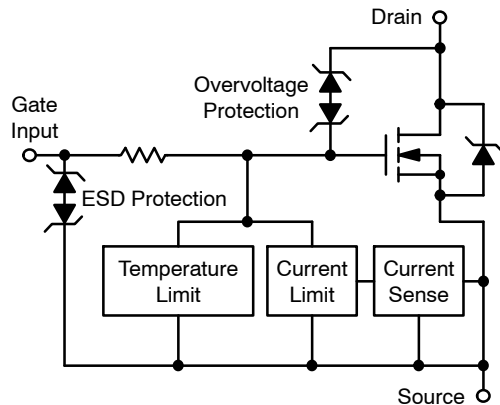
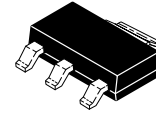


Figure 1. Block Diagram

V _{DSS} (Clamped)	R _{DS(ON)} TYP	I _D MAX (Limited)
42 V	145 mΩ @ 10 V	5.9 A

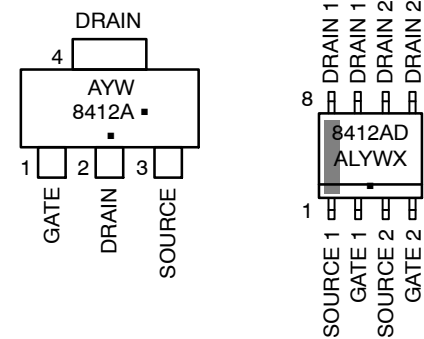


SOT-223 (TO-261)
CASE 318E



SOIC-8 NB
CASE 751

MARKING DIAGRAM



- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- 8412A or 8412AD = Specific Device Code
- = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information on page 14 of this data sheet.

NCV8412, NCV8412D

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-to-Source Voltage Internally Clamped	V_{DSS}	42	V
Drain-to-Gate Voltage Internally Clamped	V_{DG}	42	V
Gate-to-Source Voltage	V_{GS}	± 14	V
Drain Current - Continuous	I_D	Internally Limited	
Total Power Dissipation (SOT-223)	P_D	@ $T_A = 25^\circ\text{C}$ (Note 1)	1.28
		@ $T_A = 25^\circ\text{C}$ (Note 2)	2.19
Power Dissipation per Channel (SOIC-8 Dual), both channels loaded equally	P_D	@ $T_A = 25^\circ\text{C}$ (Note 1)	0.57
		@ $T_A = 25^\circ\text{C}$ (Note 2)	0.78
Total Power Dissipation (SOIC-8 Dual), only one channel loaded	P_D	@ $T_A = 25^\circ\text{C}$ (Note 1)	0.93
		@ $T_A = 25^\circ\text{C}$ (Note 2)	1.20
Thermal Resistance (SOT-223)	Junction-to-Ambient (Note 1)	$R_{\theta JA}$	97.0
	Junction-to-Ambient (Note 2)	$R_{\theta JA}$	57.0
	Junction-to-Case (Soldering Point)	$R_{\theta JS}$	7.9
Thermal Resistance (SOIC-8 Dual), both channels loaded equally	Junction-to-Ambient (Note 1)	$R_{\theta JA}$	107.8
	Junction-to-Ambient (Note 2)	$R_{\theta JA}$	79.4
	Junction-to-Case (Soldering Point)	$R_{\theta JS}$	29.0
Thermal Resistance (SOIC-8 Dual), only one channel loaded	Junction-to-Ambient (Note 1)	$R_{\theta JA}$	133.6
	Junction-to-Ambient (Note 2)	$R_{\theta JA}$	103.8
	Junction-to-Case (Soldering Point)	$R_{\theta JS}$	29.1
Single Pulse Inductive Load Switching Energy ($L = 50\text{ mH}$, $I_{L\text{peak}} = 2\text{ A}$, $V_{GS} = 5\text{ V}$, $R_G = 25\ \Omega$, $T_{J\text{start}} = 25^\circ\text{C}$)	E_{AS}	100	mJ
Load Dump Voltage ($V_{GS} = 0$ and 10 V , $R_L = 22\ \Omega$) (Note 3)	U_S^*	55	V
Operating Junction Temperature	T_J	-40 to 150	$^\circ\text{C}$
Storage Temperature	T_{storage}	-55 to 150	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- Mounted onto a 80 x 80 x 1.6 mm single layer FR4 board (100 sq mm, 1 oz. Cu, steady state)
- Mounted onto a 80 x 80 x 1.6 mm single layer FR4 board (645 sq mm, 1 oz. Cu, steady state)
- Load Dump Test B (with centralized load dump suppression) according to ISO16750-2 standard. Guaranteed by design. Not tested in production. Passed Class C according to ISO16750-1.

ESD ELECTRICAL CHARACTERISTICS (Notes 4, 5)

Parameter	Test Condition	Symbol	Min	Typ	Max	Unit
Electro-Static Discharge Capability	Human Body Model (HBM)	ESD	4000			V
	Charged Device Model (CDM)		1000			

- Not tested in production.
- This device series incorporates ESD protection and is tested by the following methods:
 ESD Human Body Model tested per AEC-Q100-002 (JS-001-2017)
 Field Induced Charge Device Model ESD characterization is not performed on plastic molded packages with body sizes smaller than 2 x 2 mm due to the inability of a small package body to acquire and retain enough charge to meet the minimum CDM discharge current waveform characteristic defined in JEDEC JS-002-2018.

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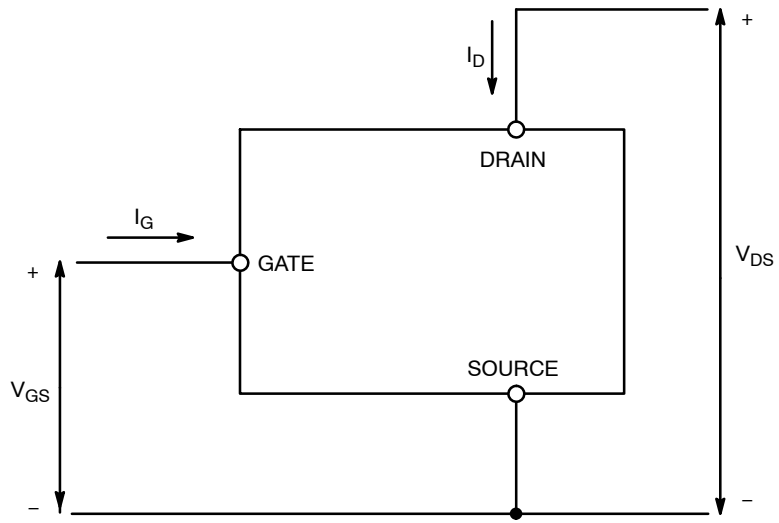


Figure 2. Voltage and Current Convention

NCV8412, NCV8412D

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Test Condition	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Clamped Breakdown Voltage	V _{GS} = 0 V, I _D = 10 mA	V _{(BR)DSS}	42	44	49	V
	V _{GS} = 0 V, I _D = 10 mA, T _J = 150°C (Note 6)		39	42	49	
Zero Gate Voltage Drain Current	V _{GS} = 0 V, V _{DS} = 32 V	I _{DSS}		0.7	4.0	μA
	V _{GS} = 0 V, V _{DS} = 32 V, T _J = 150°C (Note 6)			2.3	20	
Gate Input Current	V _{GS} = 5 V, V _{DS} = 0 V	I _{GSS}		52	72	μA

ON CHARACTERISTICS

Gate Threshold Voltage	V _{GS} = V _{DS} , I _D = 150 μA	V _{GS(th)}	1.0	1.6	2.2	V
Gate Threshold Temperature Coefficient	V _{GS} = V _{DS} , I _D = 150 μA (Note 6)	V _{GS(th)} /T _J		3.1		mV/°C
Static Drain-to-Source On Resistance	V _{GS} = 10 V, I _D = 1.7 A	R _{DS(ON)}		145	200	mΩ
	V _{GS} = 10 V, I _D = 1.7 A, T _J = 150°C (Note 6)			255	400	
	V _{GS} = 5.0 V, I _D = 1.7 A			180	230	
	V _{GS} = 5.0 V, I _D = 1.7 A, T _J = 150°C (Note 6)			310	460	
	V _{GS} = 5.0 V, I _D = 0.5 A			180	230	
	V _{GS} = 5.0 V, I _D = 0.5 A, T _J = 150°C (Note 6)			305	460	
Source-to-Drain Forward On Voltage	I _S = 7 A, V _{GS} = 0 V	V _{SD}		0.95	1.2	V

SWITCHING CHARACTERISTICS (Note 6)

Turn-On Time (10% V _{GS} to 90% I _D)	V _{GS} = 0 V to 10 V, V _{DD} = 12 V, I _D = 1 A	t _{ON}		20	31	μs
Turn-On Rise Time (10% I _D to 90% I _D)		t _{rise}		14	25	μs
Turn-Off Time (90% V _{GS} to 10% I _D)		t _{OFF}		96	140	μs
Turn-Off Fall Time (90% I _D to 10% I _D)		t _{fall}		37	50	μs
Slew Rate On (80% V _{DS} to 50% V _{DS})		-dV _{DS} /dt _{ON}	0.45	1.0		V/μs
Slew Rate Off (50% V _{DS} to 80% V _{DS})		dV _{DS} /dt _{OFF}	0.3	0.4		V/μs

SELF PROTECTION CHARACTERISTICS

Current Limit	V _{DS} = 10 V, V _{GS} = 5.0 V (Note 7)	I _{LIM}	3.3	4.4	5.6	A
	V _{DS} = 10 V, V _{GS} = 5.0 V, T _J = 150°C (Notes 6, 7)		3.3	4.0	4.9	
	V _{DS} = 10 V, V _{GS} = 10 V (Notes 6, 7)		2.6	3.9	5.9	
	V _{DS} = 10 V, V _{GS} = 10 V, T _J = 150°C (Notes 6, 7)		2.3	3.5	5.0	
Temperature Limit (Turn-Off)	V _{GS} = 5.0 V (Notes 6, 7)	T _{LIM(OFF)}	150	175	190	°C
Thermal Hysteresis		ΔT _{LIM(ON)}		15		
Temperature Limit (Turn-Off)	V _{GS} = 10 V (Notes 6, 7)	T _{LIM(OFF)}	150	185	200	
Thermal Hysteresis		ΔT _{LIM(ON)}		15		

NCV8412, NCV8412D

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Test Condition	Symbol	Min	Typ	Max	Unit
GATE INPUT CHARACTERISTICS (Note 6)						
Device ON Gate Input Current	V _{GS} = 5 V, V _{DS} = 10 V, I _D = 1 A	I _{GON}	25	52	72	μA
	V _{GS} = 10 V, V _{DS} = 10 V, I _D = 1 A		250	333	480	
Current Limit Gate Input Current	V _{GS} = 5 V, V _{DS} = 10 V	I _{GCL}	35	65	96	
	V _{GS} = 10 V, V _{DS} = 10 V		200	390	540	
Thermal Limit Gate Input Current	V _{GS} = 5 V, V _{DS} = 10 V, I _D = 0 A	I _{GTL}	550	630	750	
	V _{GS} = 10 V, V _{DS} = 10 V, I _D = 0 A		1350	1500	1650	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6. Not tested in production.

7. Refer to Application Note AND8202/D for dependence of protection features on gate voltage.

TYPICAL PERFORMANCE CURVES

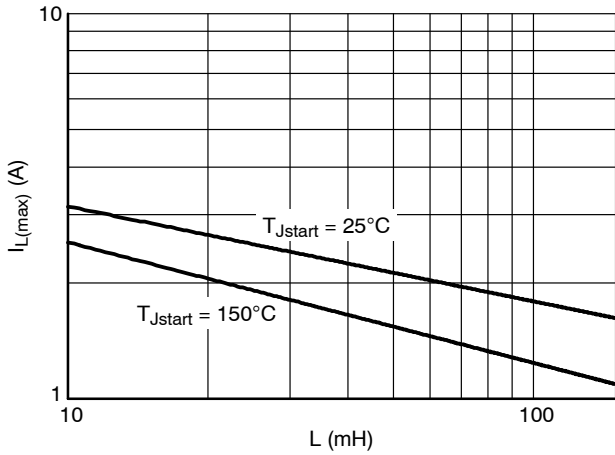


Figure 3. Single Pulse Maximum Switch-off Current vs. Load Inductance

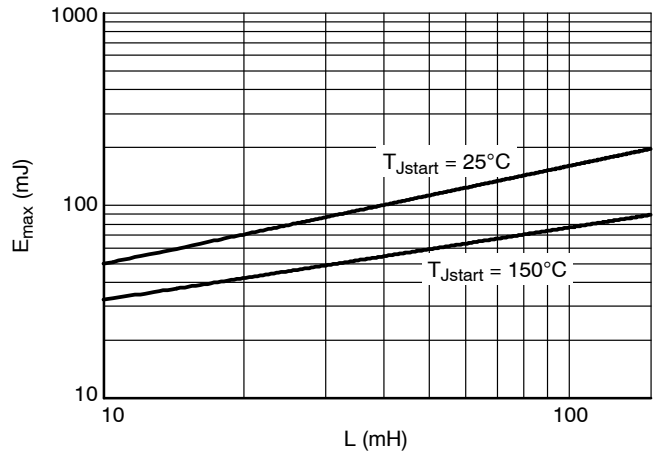


Figure 4. Single Pulse Maximum Switching Energy vs. Load Inductance

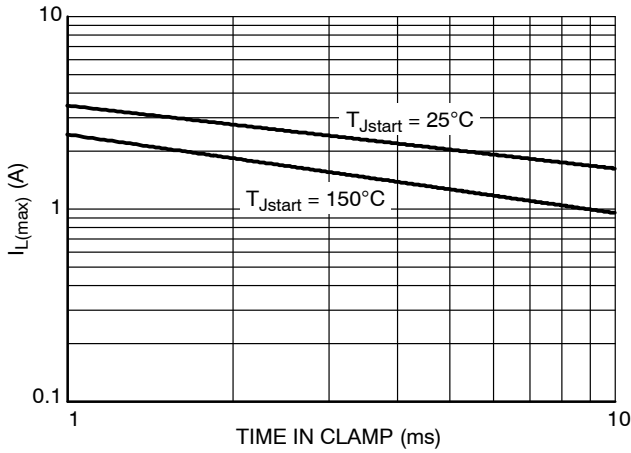


Figure 5. Single Pulse Maximum Inductive Switch-off Current vs. Time in Clamp

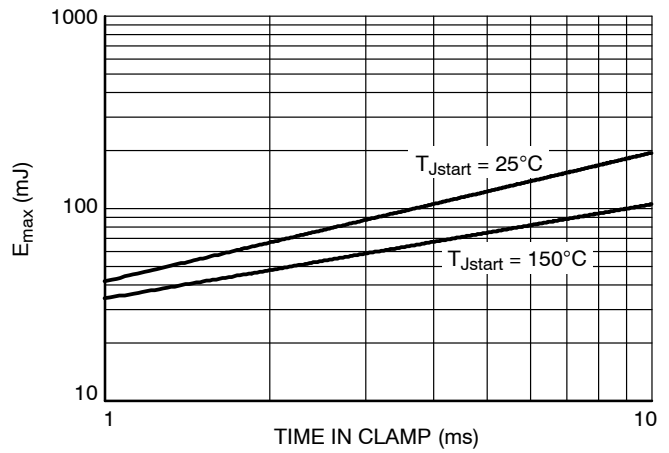


Figure 6. Single Pulse Maximum Inductive Switching Energy vs. Time in Clamp

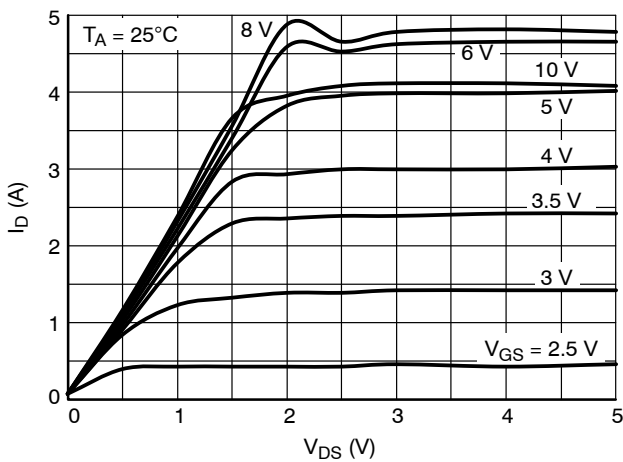


Figure 7. On-state Output Characteristics

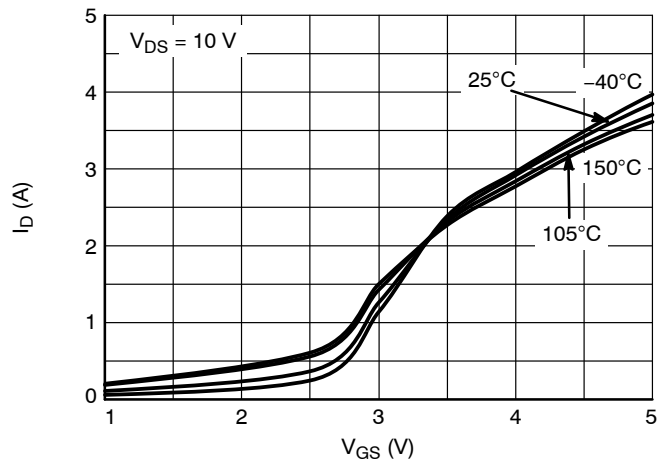


Figure 8. Transfer Characteristics

TYPICAL PERFORMANCE CURVES

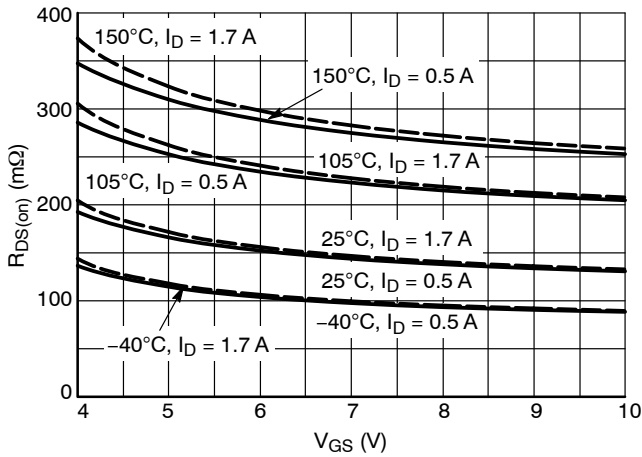


Figure 9. $R_{DS(on)}$ vs. Gate-Source Voltage

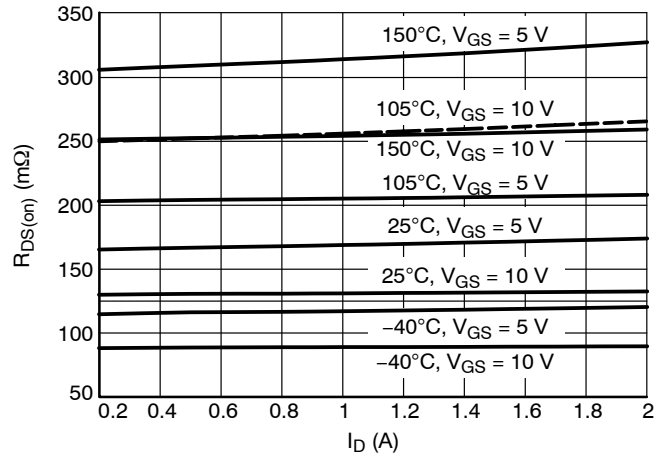


Figure 10. $R_{DS(on)}$ vs. Drain Current

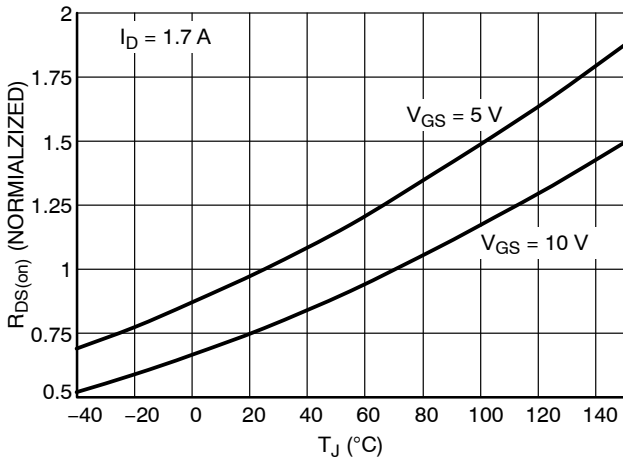


Figure 11. Normalized $R_{DS(on)}$ vs. Temperature

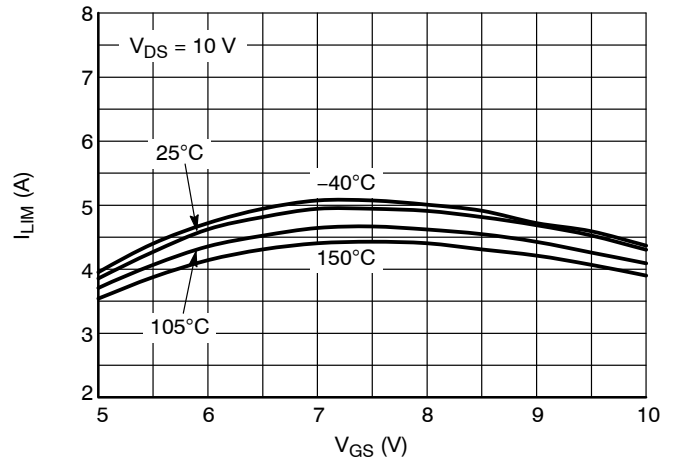


Figure 12. Current Limit vs. Gate-Source Voltage

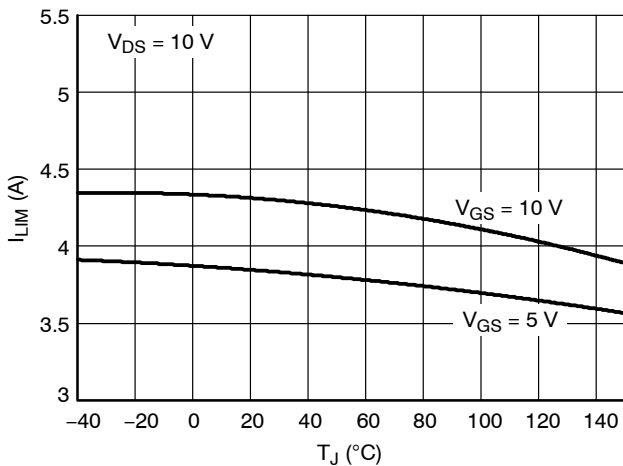


Figure 13. Current Limit vs. Junction Temperature

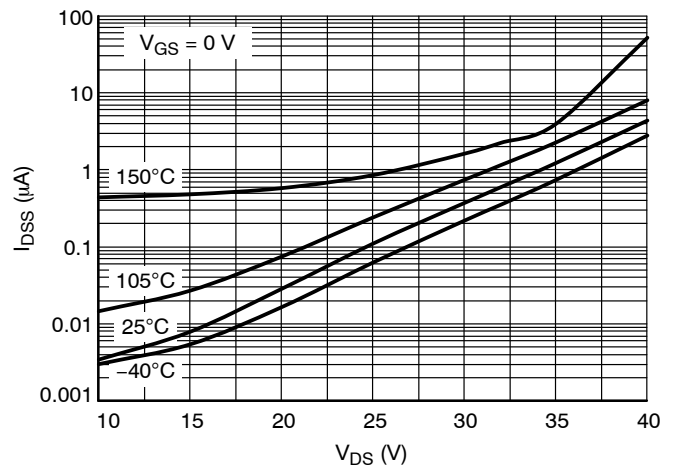


Figure 14. Drain-to-Source Leakage Current

TYPICAL PERFORMANCE CURVES

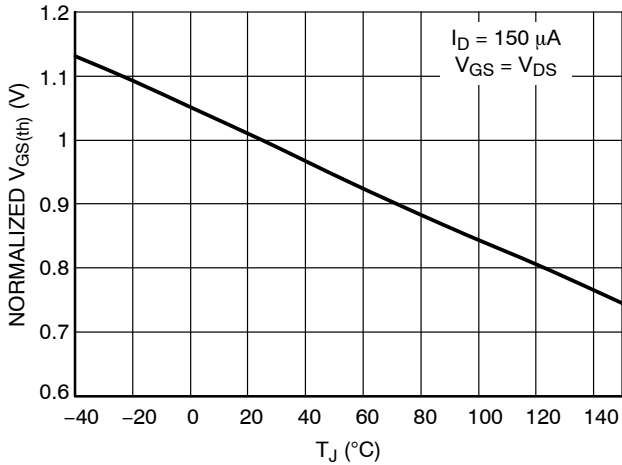


Figure 15. Normalized Threshold Voltage vs. Temperature

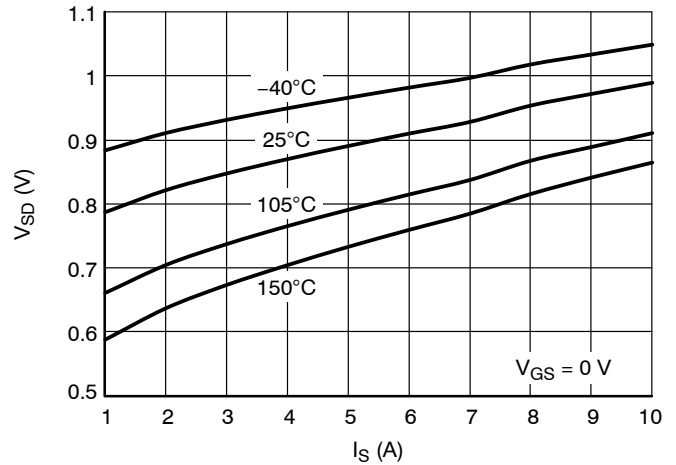


Figure 16. Source-Drain Diode Forward Characteristics

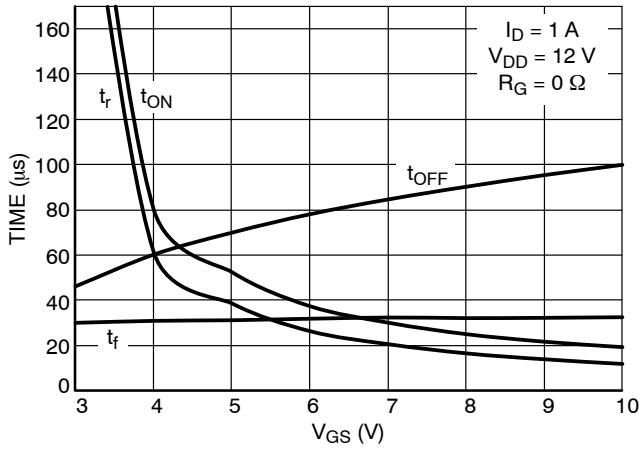


Figure 17. Resistive Load Switching Time vs. Gate-Source Voltage

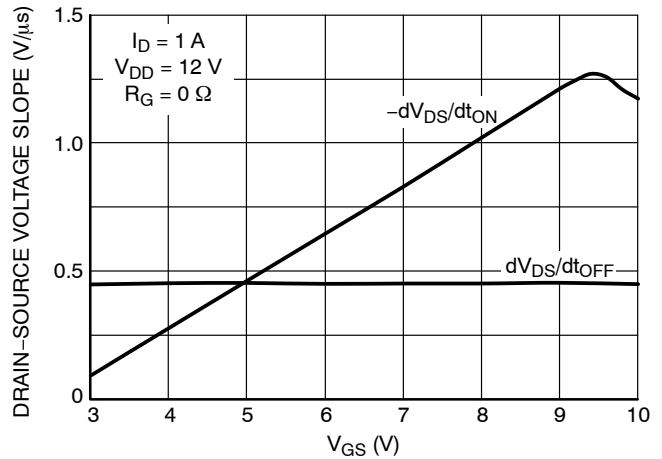


Figure 18. Resistive Load Switching Drain-Source Voltage Slope vs. Gate-Source Voltage

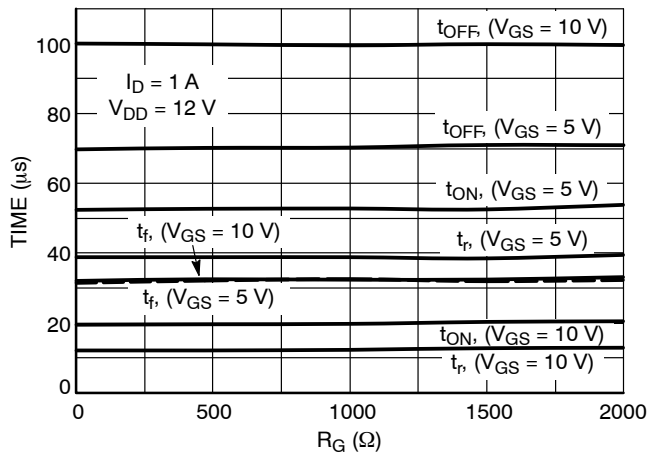


Figure 19. Resistive Load Switching Time vs. Gate Resistance

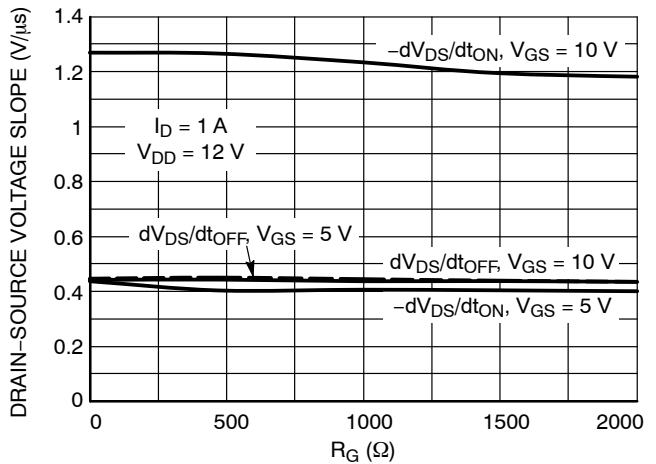


Figure 20. Drain-Source Voltage Slope during Turn On and Turn Off vs. Gate Resistance

NCV8412, NCV8412D

TYPICAL PERFORMANCE CURVES

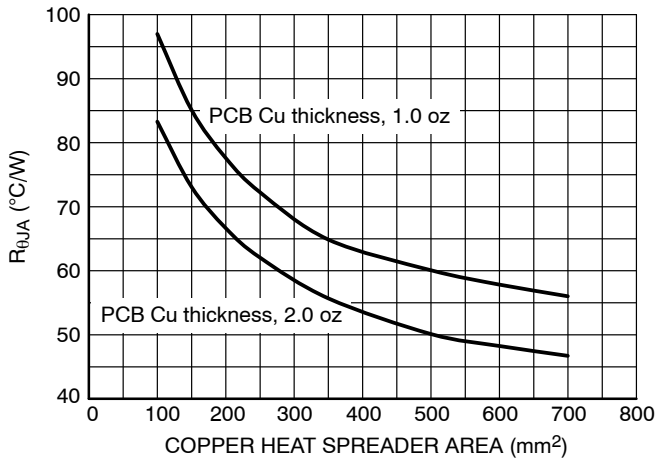


Figure 21. $R_{\theta JA}$ vs. Copper Area – SOT-223

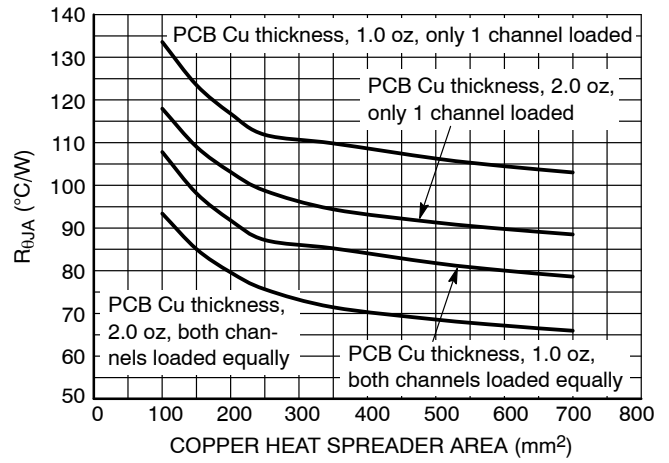


Figure 22. $R_{\theta JA}$ vs. Copper Area – SOIC-8 Dual

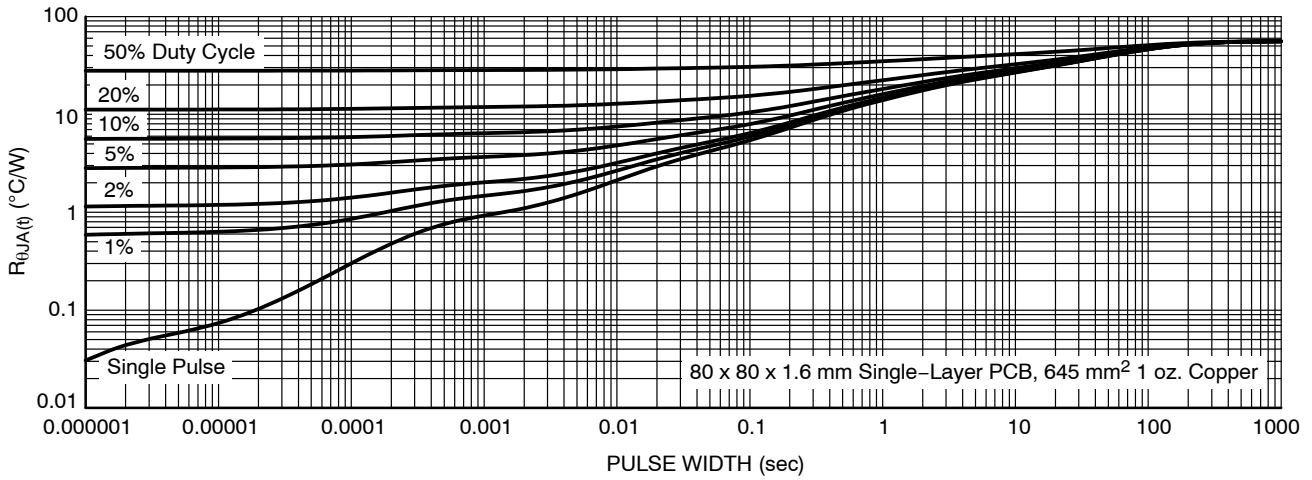


Figure 23. Transient Thermal Resistance – SOT-223

NCV8412, NCV8412D

TYPICAL PERFORMANCE CURVES

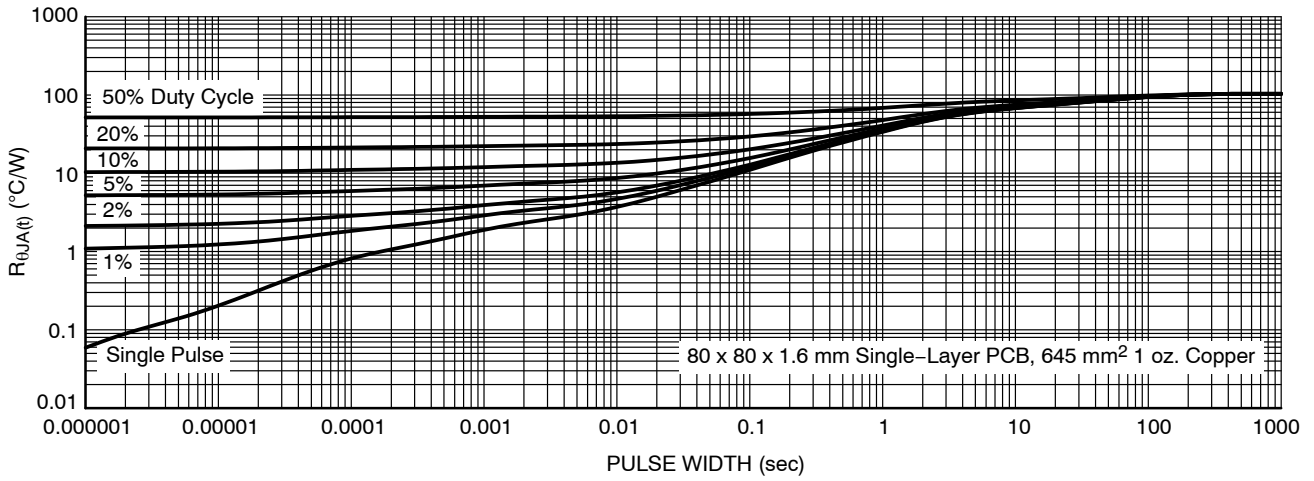


Figure 24. Transient Thermal Resistance – SOIC-8 Dual, only 1 channel loaded

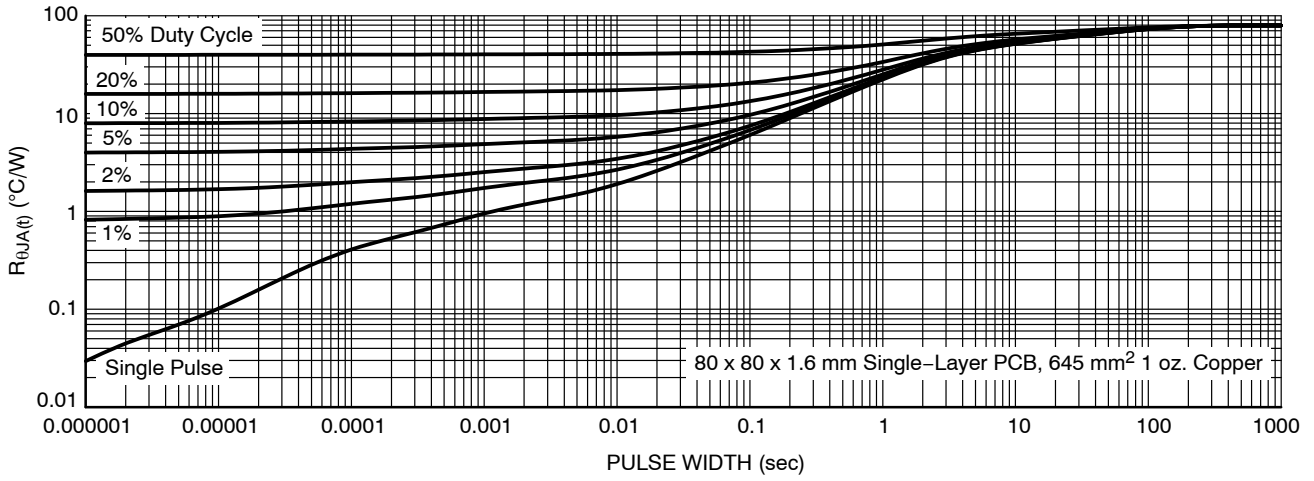


Figure 25. Transient Thermal Resistance – SOIC-8 Dual, both channels loaded equally

NCV8412, NCV8412D

APPLICATION INFORMATION

Circuit Protection Features

The NCV8412 has three main protections. Current Limit, Thermal Shutdown and Delta Thermal Shutdown. These protections establish robustness of the NCV8412.

Current Limit and Short Circuit Protection

The NCV8412 has current sense element. In the event that the drain current reaches designed current limit level, integrated Current Limit protection establishes its constant level.

Delta Thermal Shutdown

Delta Thermal Shutdown (DTSD) Protection increases higher reliability of the NCV8412. DTSD consist of two independent temperature sensors – cold and hot sensors. The NCV8412 establishes a slow junction temperature rise by sensing the difference between the hot and cold sensors. ON/OFF output cycling is designed with hysteresis that results in a controlled saw tooth temperature profile (Figure 27). The die temperature slowly rises (DTSD) until the absolute temperature shutdown (TSD) is reached around 175°C.

Thermal Shutdown with Automatic Restart

Internal Thermal Shutdown (TSD) circuitry is provided to protect the NCV8412 in the event that the maximum

junction temperature is exceeded. When activated at typically 175°C, the NCV8412 turns off. This feature is provided to prevent failures from accidental overheating.

EMC Performance

If better EMC performance is needed, connect a small ceramic capacitor to the drain pin as close to the device as possible according to Figure 26.

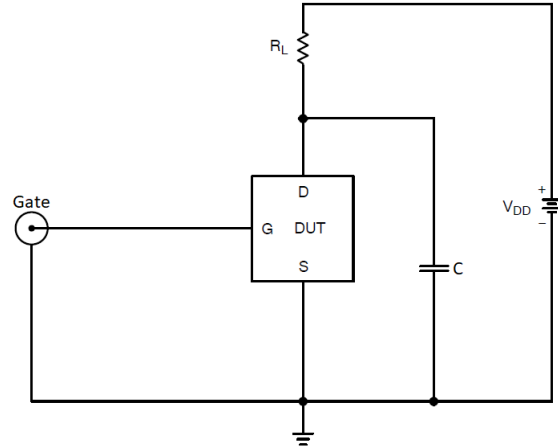


Figure 26. EMC Capacitor Placement

TEST CIRCUITS AND WAVEFORMS

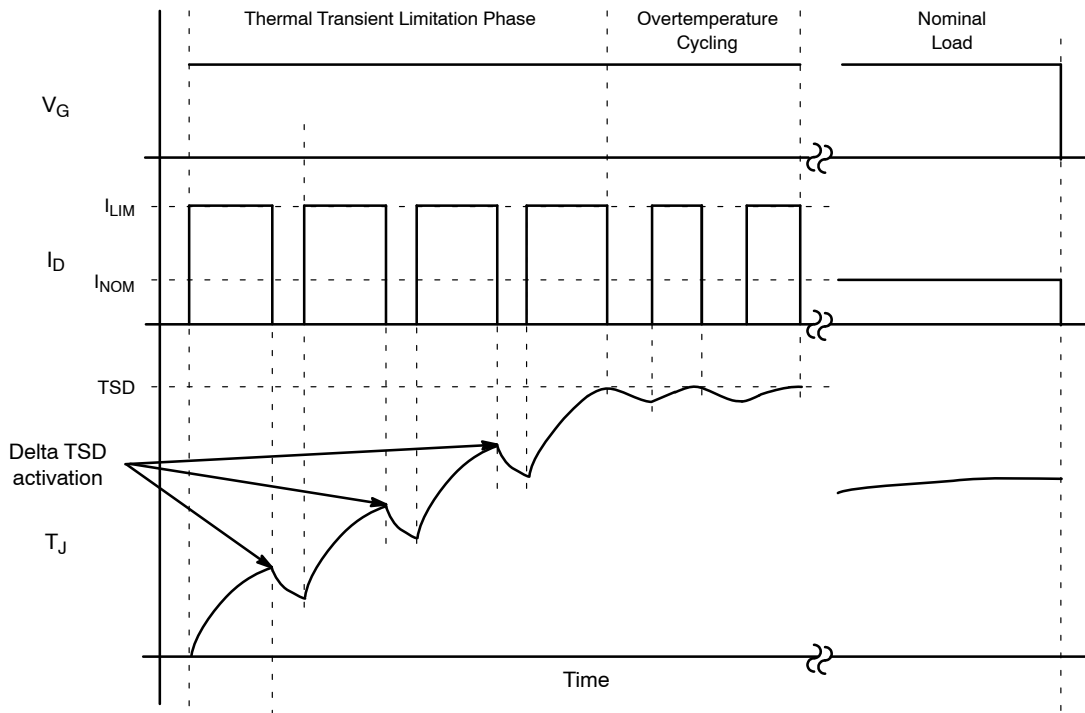


Figure 27. Overload Protection Behavior

NCV8412, NCV8412D

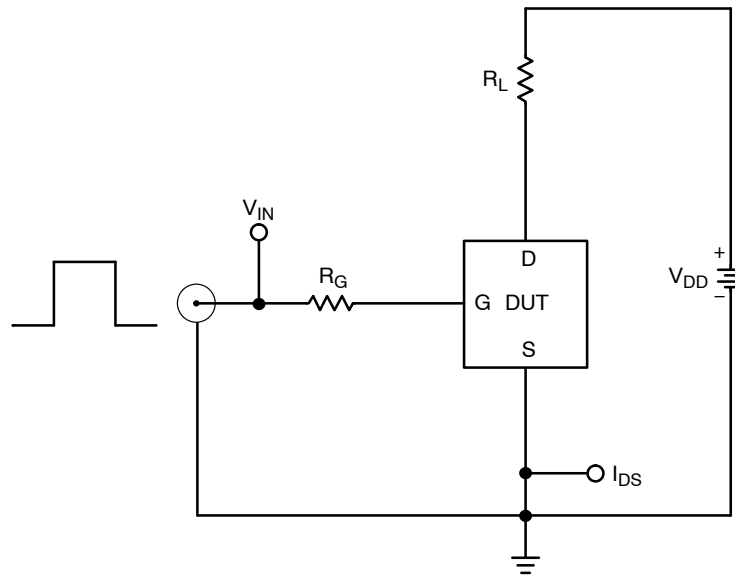


Figure 28. Resistive Load Switching Test Circuit

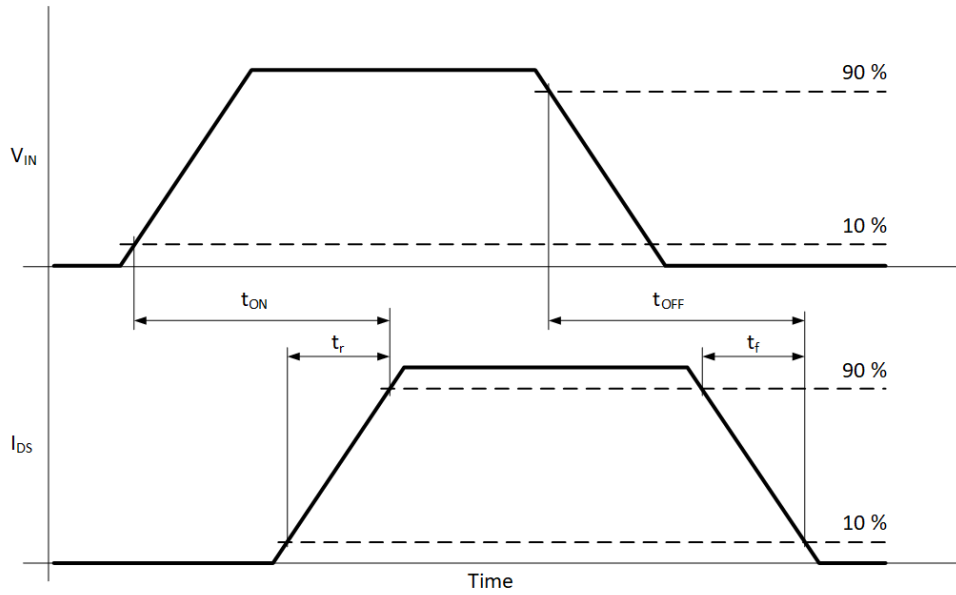


Figure 29. Resistive Load Switching Waveforms

NCV8412, NCV8412D

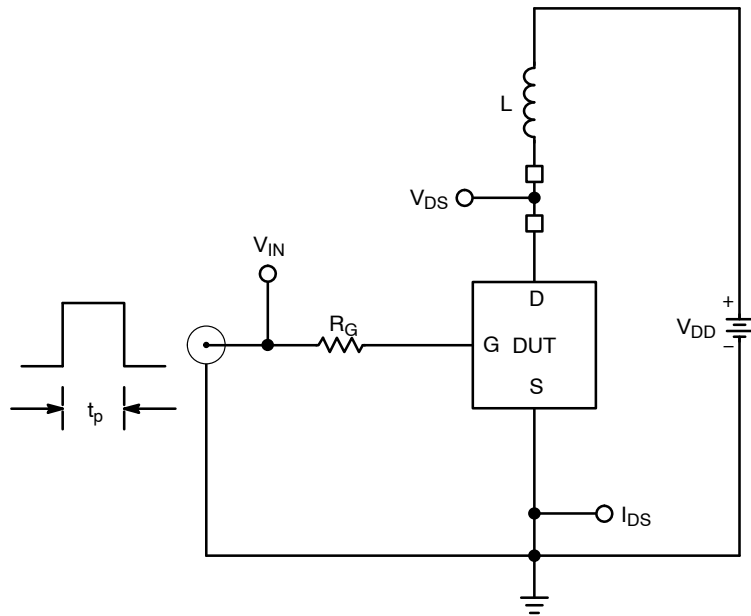


Figure 30. Inductive Load Switching Test Circuit

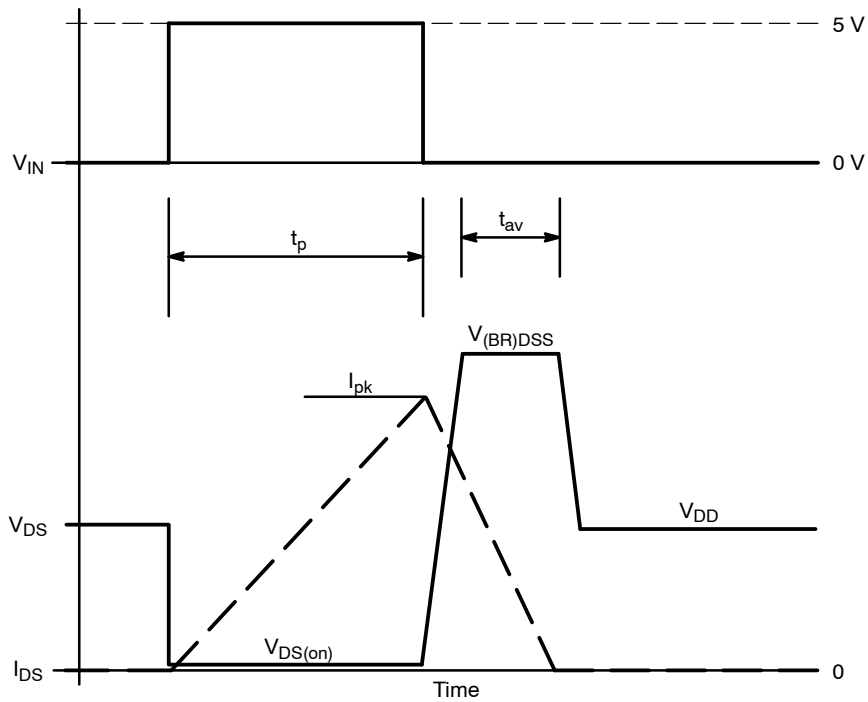


Figure 31. Inductive Load Switching Waveforms

NCV8412, NCV8412D

DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping†
NCV8412ASTT1G	8412A	SOT-223 (Pb-Free)	1,000 / Tape & Reel
NCV8412ASTT3G	8412A	SOT-223 (Pb-Free)	1,000 / Tape & Reel
NCV8412ADDR2G	8412AD	SOIC-8 (Pb-Free)	2,500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

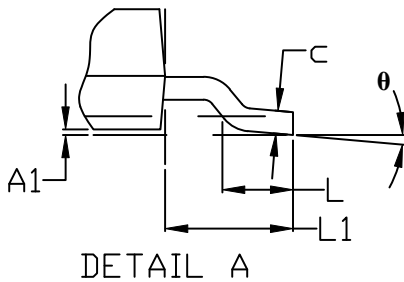
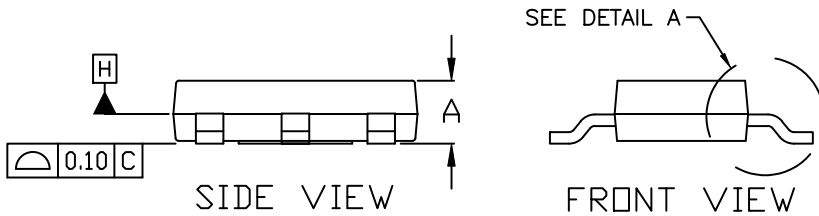
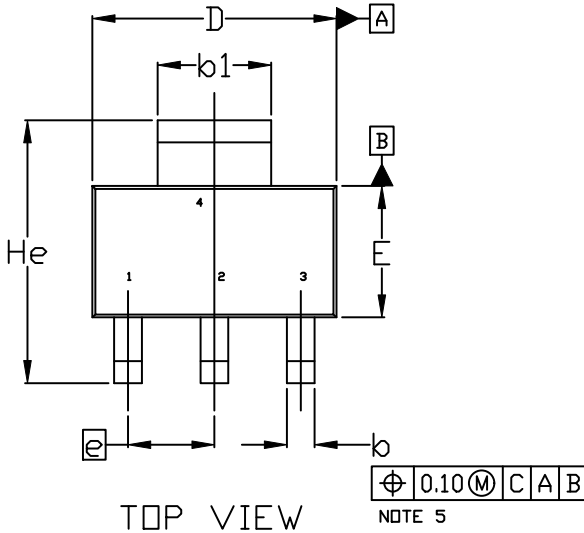
ON Semiconductor®



SCALE 1:1

SOT-223 (TO-261)
CASE 318E-04
ISSUE R

DATE 02 OCT 2018



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D & E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.200MM PER SIDE.
4. DATUMS A AND B ARE DETERMINED AT DATUM H.
5. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
6. POSITIONAL TOLERANCE APPLIES TO DIMENSIONS b AND b1.

MILLIMETERS			
DIM	MIN.	NOM.	MAX.
A	1.50	1.63	1.75
A1	0.02	0.06	0.10
b	0.60	0.75	0.89
b1	2.90	3.06	3.20
c	0.24	0.29	0.35
D	6.30	6.50	6.70
E	3.30	3.50	3.70
e	2.30 BSC		
L	0.20	---	---
L1	1.50	1.75	2.00
He	6.70	7.00	7.30
θ	0°	---	10°



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ISSUE R

DATE 02 OCT 2018

- | | | | | |
|--|---|---|---|---|
| STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR | STYLE 2:
PIN 1. ANODE
2. CATHODE
3. NC
4. CATHODE | STYLE 3:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN | STYLE 4:
PIN 1. SOURCE
2. DRAIN
3. GATE
4. DRAIN | STYLE 5:
PIN 1. DRAIN
2. GATE
3. SOURCE
4. GATE |
| STYLE 6:
PIN 1. RETURN
2. INPUT
3. OUTPUT
4. INPUT | STYLE 7:
PIN 1. ANODE 1
2. CATHODE
3. ANODE 2
4. CATHODE | STYLE 8:
CANCELLED | STYLE 9:
PIN 1. INPUT
2. GROUND
3. LOGIC
4. GROUND | STYLE 10:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE |
| STYLE 11:
PIN 1. MT 1
2. MT 2
3. GATE
4. MT 2 | STYLE 12:
PIN 1. INPUT
2. OUTPUT
3. NC
4. OUTPUT | STYLE 13:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR | | |

**GENERIC
 MARKING DIAGRAM***




- A = Assembly Location
- Y = Year
- W = Work Week
- XXXXX = Specific Device Code
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	SOT-223 (TO-261)	PAGE 2 OF 2

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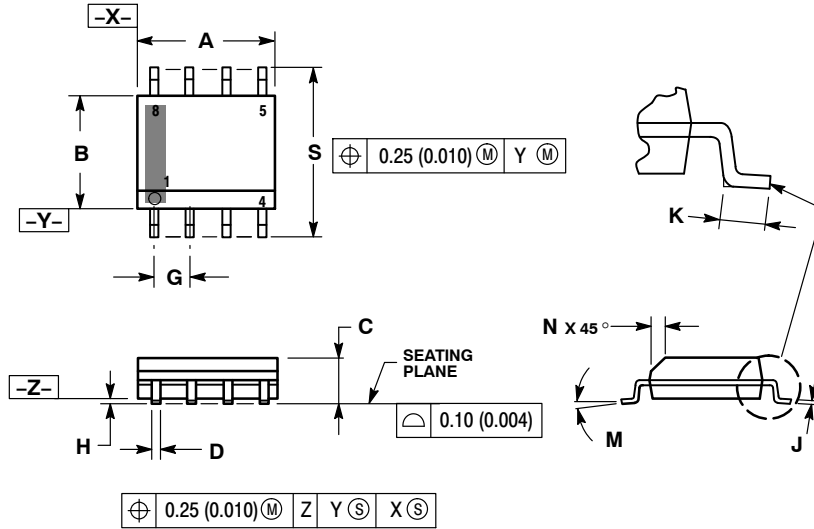
MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1

SOIC-8 NB
CASE 751-07
ISSUE AK

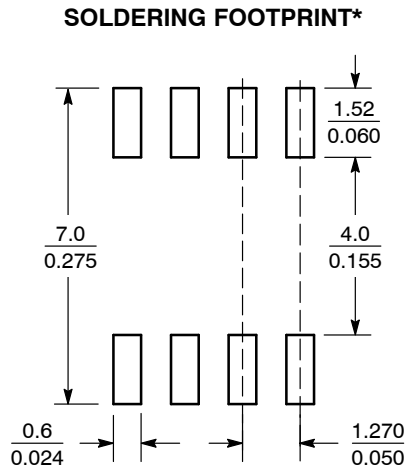
DATE 16 FEB 2011



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
 5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
 6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

GENERIC MARKING DIAGRAM*



SCALE 6:1 ($\frac{\text{mm}}{\text{inches}}$)



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

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SOIC-8 NB
CASE 751-07
ISSUE AK

DATE 16 FEB 2011

- | | | | |
|---|--|--|--|
| <p>STYLE 1:
 PIN 1. EMITTER
 2. COLLECTOR
 3. COLLECTOR
 4. EMITTER
 5. EMITTER
 6. BASE
 7. BASE
 8. EMITTER</p> | <p>STYLE 2:
 PIN 1. COLLECTOR, DIE, #1
 2. COLLECTOR, #1
 3. COLLECTOR, #2
 4. COLLECTOR, #2
 5. BASE, #2
 6. EMITTER, #2
 7. BASE, #1
 8. EMITTER, #1</p> | <p>STYLE 3:
 PIN 1. DRAIN, DIE #1
 2. DRAIN, #1
 3. DRAIN, #2
 4. DRAIN, #2
 5. GATE, #2
 6. SOURCE, #2
 7. GATE, #1
 8. SOURCE, #1</p> | <p>STYLE 4:
 PIN 1. ANODE
 2. ANODE
 3. ANODE
 4. ANODE
 5. ANODE
 6. ANODE
 7. ANODE
 8. COMMON CATHODE</p> |
| <p>STYLE 5:
 PIN 1. DRAIN
 2. DRAIN
 3. DRAIN
 4. DRAIN
 5. GATE
 6. GATE
 7. SOURCE
 8. SOURCE</p> | <p>STYLE 6:
 PIN 1. SOURCE
 2. DRAIN
 3. DRAIN
 4. SOURCE
 5. SOURCE
 6. GATE
 7. GATE
 8. SOURCE</p> | <p>STYLE 7:
 PIN 1. INPUT
 2. EXTERNAL BYPASS
 3. THIRD STAGE SOURCE
 4. GROUND
 5. DRAIN
 6. GATE 3
 7. SECOND STAGE Vd
 8. FIRST STAGE Vd</p> | <p>STYLE 8:
 PIN 1. COLLECTOR, DIE #1
 2. BASE, #1
 3. BASE, #2
 4. COLLECTOR, #2
 5. COLLECTOR, #2
 6. EMITTER, #2
 7. EMITTER, #1
 8. COLLECTOR, #1</p> |
| <p>STYLE 9:
 PIN 1. EMITTER, COMMON
 2. COLLECTOR, DIE #1
 3. COLLECTOR, DIE #2
 4. EMITTER, COMMON
 5. EMITTER, COMMON
 6. BASE, DIE #2
 7. BASE, DIE #1
 8. EMITTER, COMMON</p> | <p>STYLE 10:
 PIN 1. GROUND
 2. BIAS 1
 3. OUTPUT
 4. GROUND
 5. GROUND
 6. BIAS 2
 7. INPUT
 8. GROUND</p> | <p>STYLE 11:
 PIN 1. SOURCE 1
 2. GATE 1
 3. SOURCE 2
 4. GATE 2
 5. DRAIN 2
 6. DRAIN 2
 7. DRAIN 1
 8. DRAIN 1</p> | <p>STYLE 12:
 PIN 1. SOURCE
 2. SOURCE
 3. SOURCE
 4. GATE
 5. DRAIN
 6. DRAIN
 7. DRAIN
 8. DRAIN</p> |
| <p>STYLE 13:
 PIN 1. N.C.
 2. SOURCE
 3. SOURCE
 4. GATE
 5. DRAIN
 6. DRAIN
 7. DRAIN
 8. DRAIN</p> | <p>STYLE 14:
 PIN 1. N-SOURCE
 2. N-GATE
 3. P-SOURCE
 4. P-GATE
 5. P-DRAIN
 6. P-DRAIN
 7. N-DRAIN
 8. N-DRAIN</p> | <p>STYLE 15:
 PIN 1. ANODE 1
 2. ANODE 1
 3. ANODE 1
 4. ANODE 1
 5. CATHODE, COMMON
 6. CATHODE, COMMON
 7. CATHODE, COMMON
 8. CATHODE, COMMON</p> | <p>STYLE 16:
 PIN 1. EMITTER, DIE #1
 2. BASE, DIE #1
 3. EMITTER, DIE #2
 4. BASE, DIE #2
 5. COLLECTOR, DIE #2
 6. COLLECTOR, DIE #2
 7. COLLECTOR, DIE #1
 8. COLLECTOR, DIE #1</p> |
| <p>STYLE 17:
 PIN 1. VCC
 2. V2OUT
 3. V1OUT
 4. TXE
 5. RXE
 6. VEE
 7. GND
 8. ACC</p> | <p>STYLE 18:
 PIN 1. ANODE
 2. ANODE
 3. SOURCE
 4. GATE
 5. DRAIN
 6. DRAIN
 7. CATHODE
 8. CATHODE</p> | <p>STYLE 19:
 PIN 1. SOURCE 1
 2. GATE 1
 3. SOURCE 2
 4. GATE 2
 5. DRAIN 2
 6. MIRROR 2
 7. DRAIN 1
 8. MIRROR 1</p> | <p>STYLE 20:
 PIN 1. SOURCE (N)
 2. GATE (N)
 3. SOURCE (P)
 4. GATE (P)
 5. DRAIN
 6. DRAIN
 7. DRAIN
 8. DRAIN</p> |
| <p>STYLE 21:
 PIN 1. CATHODE 1
 2. CATHODE 2
 3. CATHODE 3
 4. CATHODE 4
 5. CATHODE 5
 6. COMMON ANODE
 7. COMMON ANODE
 8. CATHODE 6</p> | <p>STYLE 22:
 PIN 1. I/O LINE 1
 2. COMMON CATHODE/VCC
 3. COMMON CATHODE/VCC
 4. I/O LINE 3
 5. COMMON ANODE/GND
 6. I/O LINE 4
 7. I/O LINE 5
 8. COMMON ANODE/GND</p> | <p>STYLE 23:
 PIN 1. LINE 1 IN
 2. COMMON ANODE/GND
 3. COMMON ANODE/GND
 4. LINE 2 IN
 5. LINE 2 OUT
 6. COMMON ANODE/GND
 7. COMMON ANODE/GND
 8. LINE 1 OUT</p> | <p>STYLE 24:
 PIN 1. BASE
 2. EMITTER
 3. COLLECTOR/ANODE
 4. COLLECTOR/ANODE
 5. CATHODE
 6. CATHODE
 7. COLLECTOR/ANODE
 8. COLLECTOR/ANODE</p> |
| <p>STYLE 25:
 PIN 1. VIN
 2. N/C
 3. REXT
 4. GND
 5. IOUT
 6. IOUT
 7. IOUT
 8. IOUT</p> | <p>STYLE 26:
 PIN 1. GND
 2. dv/dt
 3. ENABLE
 4. ILIMIT
 5. SOURCE
 6. SOURCE
 7. SOURCE
 8. VCC</p> | <p>STYLE 27:
 PIN 1. ILIMIT
 2. OVLO
 3. UVLO
 4. INPUT+
 5. SOURCE
 6. SOURCE
 7. SOURCE
 8. DRAIN</p> | <p>STYLE 28:
 PIN 1. SW_TO_GND
 2. DASIC_OFF
 3. DASIC_SW_DET
 4. GND
 5. V_MON
 6. VBULK
 7. VBULK
 8. VIN</p> |
| <p>STYLE 29:
 PIN 1. BASE, DIE #1
 2. EMITTER, #1
 3. BASE, #2
 4. EMITTER, #2
 5. COLLECTOR, #2
 6. COLLECTOR, #2
 7. COLLECTOR, #1
 8. COLLECTOR, #1</p> | <p>STYLE 30:
 PIN 1. DRAIN 1
 2. DRAIN 1
 3. GATE 2
 4. SOURCE 2
 5. SOURCE 1/DRAIN 2
 6. SOURCE 1/DRAIN 2
 7. SOURCE 1/DRAIN 2
 8. GATE 1</p> | | |

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